ABSTRACT

A method for monitoring fabrication of an integrated circuit (IC) on a semiconductor wafer includes generating a product design profile (PDP) using an electronic design automation (EDA) tool, the PDP comprising an indication of a site in at least one layer of the IC that is susceptible to a process fault. Upon fabricating at least one layer of the IC on the wafer, a process monitoring tool is applied to perform a measurement at the site in at least one layer responsively to the PDP.